13 15. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

said semiconductor device including an inner area at a surface, an input/output area surrounding said inner area therein, and a pad area surrounding said input/output area therein,

said semiconductor device including a plurality of input/output terminals in said input/output area, and a plurality of pads in said pad area,

said semiconductor device including (a) a first source voltage wire being electrically connected to a voltage source and surrounding said inner area in said pad area, and (b) a first ground wire being grounded and surrounding said first source voltage wire in said pad area,

A5 cont

each of said pads being electrically connected to any one of said input/output terminals, said first source voltage wire, and said first ground wire,

said semiconductor device including a protection device fabricated below said pad area,

said protection device comprising:

(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on second interlayer insulating film,

said first layer including a first metal wiring layer, a second metal wiring layer, and a second signal wiring layer all electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal wiring layer through via-holes formed through said second interlayer insulating film.

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~~16~~. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

A5 cont

said semiconductor device including an inner area at a surface, an input/output area surrounding said inner area therein, and a pad area surrounding said input/output area therein,

said semiconductor device including a plurality of input/output terminals in said input/output area, and a plurality of pads in said pad area,

said semiconductor device including (a) a first source voltage wire being electrically connected to a voltage source and surrounding said inner area in said pad area, and (b) a first ground wire being grounded and surrounding said first source voltage wire in said pad area,

each of said pads being electrically connected to any one of said input/output terminals, said first source voltage wire, and said first ground wire,

said input/output area having an extended portion located below said pad area,

said extended portion comprising:

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(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on second interlayer insulating film,

said first layer including a first metal wiring layer electrically connected to said first well through a via-hole formed through said first interlayer insulating film, a second metal wiring layer electrically connected to said second well through a via-hole formed through said first interlayer insulating film, and a second signal wiring layer electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal wiring layer through via-holes formed through said second interlayer insulating film.

Please add the following new claims:

22. (New) The semiconductor device as set forth in claim 1, wherein said device comprises a bypass capacitor.

23. (New) The semiconductor device as set forth in claim 1, wherein said device comprises a protection device.

24. (New) The semiconductor device as set forth in claim 1, wherein said device comprises an input/output device.

25. (New) The semiconductor device as set forth in claim 1, further comprising a second device fabricated below said device,

said device comprises a bypass capacitor,

said second device comprises a protection device.

26. (New) The semiconductor device as set forth in claim 1, further comprising a second device fabricated below said device,

said device comprises a bypass capacitor,

said second device comprises an input/output device.

27. (New) The semiconductor device as set forth in claim 22, wherein said bypass capacitor comprises metal wire layers arranged below said pad area.

28. (New) The semiconductor device as set forth in claim 27, wherein each of said metal wire layers comprises a first wire and a second wire with an interlayer insulating layer being sandwiched therebetween,

said first wire being electrically connected to a voltage source,

said second wire being grounded.

29. (New) The semiconductor device as set forth in claim 27, wherein each of said metal wire layers comprises a first comb-shaped wire being electrically connected to a voltage source and a second comb-shaped wire being grounded,

said first and second wires being arranged such that teeth of said first comb-shaped wire are located between teeth of said second comb-shaped wire in the same plane.

30. (New) The semiconductor device as set forth in claim 28, further comprising at least one of first to fourth pads in said pad area,

said first pad being electrically connected to an input/output device,

said second pad being electrically connected to said first wire,

said third pad being electrically connected to said second wire,

said fourth pad being not electrically connected to said input/output device, said first wire and said second wire.